A New Decoder-type Gate Driver Circuit for High Resolution

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These days, the display has various form factors which are flexible, foldable, and stretchable [1]. Due to the physical stress, the reliability of the gate driver circuit should be considered. However, the fault of one stage is fatal in the conventional shift register-type gate driver circuit, because it causes a malfunction in the whole subsequent stages. To solve this problem, decoder-type gate driver circuits had been proposed [2]. Because each stage operates independently, the effect of fault can be minimized. However, unlike the conventional gate driver, the number of signals of the decoder-type gate driver should be increased according to the resolution of the display. Thus it is difficult to apply to high resolution like FHD and 4k UHD.

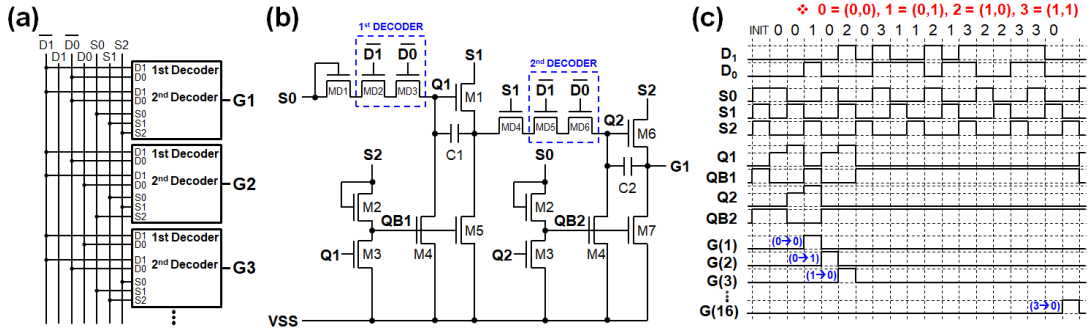
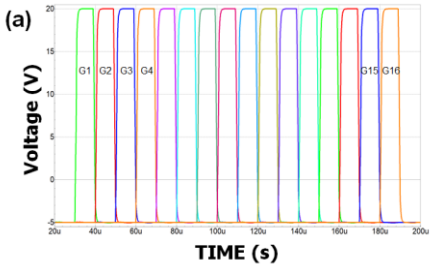


Fig. 1. (a) Block diagram, (b) circuit diagram of unit stage and (c) timing diagram of proposed gate driver.

To overcome this problem, we propose a new decoder-type gate driver as shown in Fig. 1. The unit stage of the proposed circuit consists of two decoding stages. Instead of using different decoder signals in two decoding stages, we use the same decoder signals which are distinguished by the timing. The input signal is transmitted to the next stage only when the decoder is open at the same timing of the input signal. Thus gate voltage is only output when the 1st and 2nd decoder stage sequentially operates. Moreover, the gate output voltage has no blank timing by using the same decoder signal between the 2nd decoding stage of the previous stage and the 1st decoding stage of the next stage.



(b)

STAGE #	2 STAGE					3 STAGE		
DECODER #	2	3	4	5	6	2	3	4
OUTPUT #	16	64	256	1024	4096	64	512	4096
SIGNAL #	8	10	12	14	16	8	10	12
TR #	16	18	20	22	24	24	27	30

This paper

Fig. 2. (a) Simulation results and (b) comparison according to number of decoder signals and stages.

Fig. 2(a) shows simluation results of 16 stage of proposed gate driver. And as shown in Fig. 2(b), proposed circuit use 16 signals and 24 transistors to drive FHD resolution while conventional decoder-type gate driver uses 23 signals and 21 transisotrs [2].

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