Fault-Tolerant Integrated Gate Driver for Flexible Displays

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Abstract

This paper proposes a fault-tolerant integrated gate driver for flexible displays. To achieve fault-tolerance, decoder-type gate driver circuit is chosen. Fault detection circuit and redundant circuits are also added. The function of the proposed circuit is verified by simulation and fabrication results. The measurement results of the proposed gate driver with 16 stages on PI substrate comprising a-IGZO TFT is presented.

Author Keywords

Flexible display; gate driver; fault-tolerance; redundancy;

1. Introduction

As display technology improves, various form factors of display have appeared which are flexible, foldable and stretchable [1-3]. Because there could be continuous and repetitive physical stress, it is important to have high reliability against it. In that sense, high reliability of the gate driver circuit is also required because they used to be integrated on the display substrate for achieving narrow bezel and low cost [4-5]. Moreover, the fault of the gate driver circuit is fatal compared to other parts of the display because the fault of one stage causes a malfunction in the whole subsequent stages. Therefore, it is highly demanded the circuit which can tolerate the faults.

In this paper, we propose the fault-tolerant integrated gate driver circuit including fault detection circuit and redundant unit. If a fault occurs, it can be detected by the fault detection circuit and the stage where the fault occurs will be replaced with the redundant unit. Although the proposed circuit occupies more area than the conventional one, it has the advantage to offset its drawback in terms of increasing the lifetime of the panel.
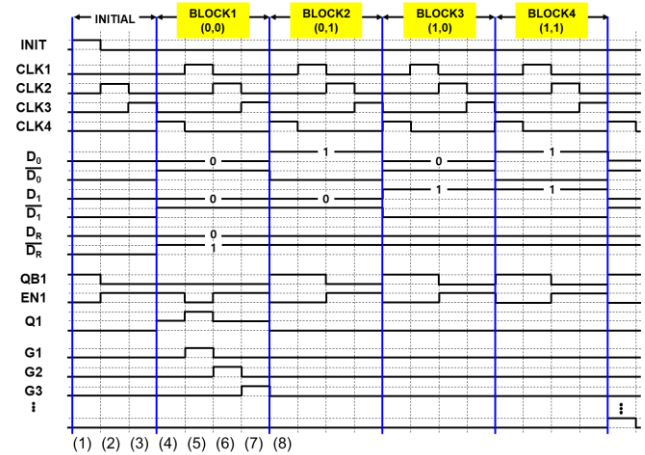
2. Proposed gate driver circuit

Unlike a carry-type gate driver circuit, a decoder-type gate driver operates independently stage by stage [6]. In addition, we add the fault detection circuit [7] and redundant unit to achieve fault-tolerant architecture. Figure 1 shows circuit diagram and timing diagram of unit stage of proposed gate driver circuit. And Fig. 2 shows the overall architecture.

Initialize: The operation of the proposed circuit, for example stage1, is as follows. In the period (1), QB nodes of all stages are charged via transistor M7. This prevents the output voltage from the unselected blocks. In the period (2), the EN node is charged via transistor M3 when CLK2 rises to a high level. Although the EN node is discharged at the same time by M5 which is turned on by the QB node, it can be charged because the size of M3 is bigger than that of M5. The EN node turns on the transistor M10 and it discharges the QB node. And there is no change in period (3).
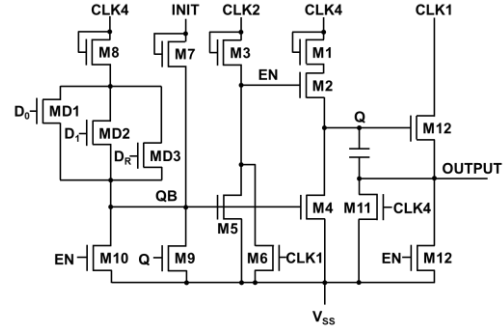
(a) Circuit diagram of unit stage of proposed gate driver circuit.

(b) Timing diagram of the proposed gate driver circuit.

Figure 1. Circuit diagram (a) and timing diagram (b) of proposed gate driver circuit.

Decoder-Selected: During the period between (4) and (7), block1 is in the decoder-selected state which means transistor MD1-MD3 are turned off by decoder signals. Thus the QB node keeps low state although CLK4 rises to a high level in the period (4). Because the EN node is not discharged by the QB node, the Q node can be charged by series of transistor M1 and M2. In the period (5), when CLK1 rises to a high level, the Q node voltage rises much higher than a supply voltage by bootstrapping with the OUTPUT node. Therefore the OUTPUT node can be charged without voltage drop. Meanwhile, the EN node is discharged to turn off the pull down transistor M12. In the period (6), CLK1 falls to a low level with the Q node is still charged. Because the size of the transistor M12 is large, the OUTPUT node voltage can be discharged rapidly. Also, the EN node is charged by CLK2, transistor M12 pulls down the OUTPUT node during the period (6) and (7).
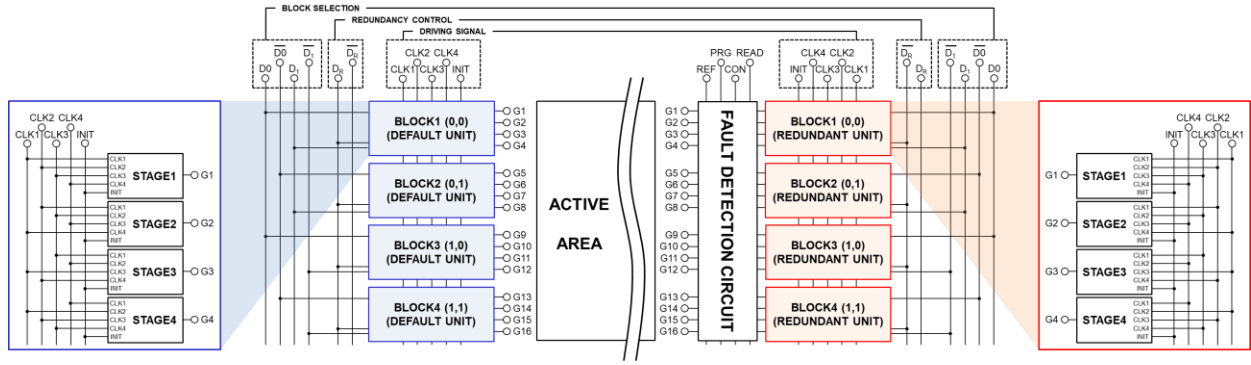
Figure 2. Overall architecture of the proposed gate driver circuit with redundant unit.

Decoder-Unselected: Since period (8), the block1 remains decoder-unselected state which means at least one of the transistor among MD1-MD3 are turned on by decoder signals. For example, when CLK4 rises to a high level in the period (8), the QB node is charged by the transistor MD1. Transistor M8 and MD1-MD3 have a size large enough to charge QB node while they are discharged by M10. The QB node keeps the Q node and the EN node to a low level through transistor M4 and M5 respectively. This prevents the OUTPUT voltage from unselected blocks. However, unlike other conventional circuits [4-5], the QB node does not pull down the OUTPUT node. If it does, output voltages from the decoder-selected block could be pulled down by its redundant circuit whose QB node is charged. Instead, transistor M11 and transistor M12 pulls down the OUTPUT node in the period (8) and (9)-(10) respectively. Because all the pull-down transistors are not turned on constantly but turned on periodically, it can reduce the voltage stress of transistors.

Fault Detection: The operation of the fault-tolerant system is as follows. Each gate output voltage determines whether or not to transmit the reference signal to the readout node. If there is a fault in gate driver output, it can be detected by comparing the readout voltage with reference signal and the stage where the fault occurs will be replaced with the redundant unit. The threshold level of gate output voltage which triggers the circuits can be programmed. Detail of the detection circuit is in our previous works [7].

Redundancy Control: For an example of stage1, decoder signal changes in the period (4) determine whether to drive a default circuit or a redundant circuit in the period (5) because whether the QB node is charged or not is changed. The transistor M9 and M10 prevent the effect of capacitive coupling that can be caused by changing the decoder signal in other timing.

3. Results and Discussion

Table1 shows simulation parameters and Fig. 3 shows following results. The simulation result shows that the output voltages were reached VDD voltage and sequentially output according to the decoder signal. In addition, we simulated the proposed circuit alternating between default and redundant circuits to verify the redundancy control of the proposed circuit. Although only one Q node of the two units is charged at the same time, the gate output voltage of all stages operates normally as shown in Fig.3. This means redundancy of the gate driver circuit can be controlled in any period without malfunction.

Table 1. Simulation parameters

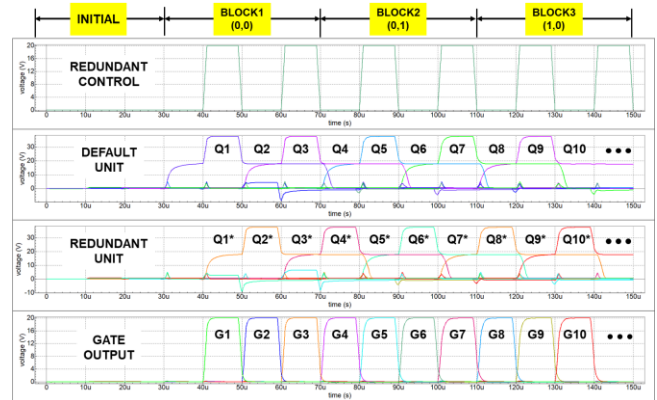| R_{LOAD}, C_{LOAD}	5kΩ, 120pF
VDD, VSS	20V, 0V
C1	2pF
Pulse Width	10μs
Backplane	a-IGZO
M1, M2, M3, M7, M8, M12, MD1, MD2, MD3	W/L = (40μm/10μm)
M4, M5	W/L = (20μm/10μm)
M6, M9, M10, M11	W/L = (10μm/10μm)
M12	W/L = (1000μm/10μm)

Figure 3. Simulation results of proposed gate driver circuit.

16 stage of the proposed gate driver circuit with redundant unit and fault detection circuit were fabricated on PI substrate and the Fig.4 shows the layout. The gate driver circuit occupies 529μm by 1,286μm per stage and two units were fabricated. There is a tradeoff between the number of gate driver units and the total area of gate driver which is closely related to the size of the bezel. And the fault detection unit occupies 529μm by 744μm per stage.
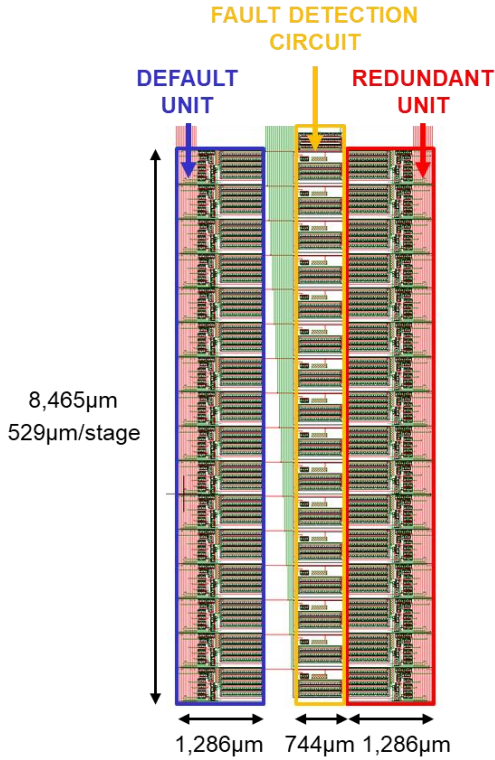
Figure 4. Layout of the 16 stage of proposed gate driver circuit including redundant unit and fault detection circuit.

Fig. 5 shows the transfer curve of a-IGZO TFT. As shown in the graph, characteristics of the fabricated circuit are different from the expected characteristics which were used in simulation results. As threshold voltage is shifted to a negative direction, the fabricated circuit operates in depletion mode, not enhancement mode. As a result, a leakage current occurs in the QB node and it causes a ripple voltage of gate output voltage.
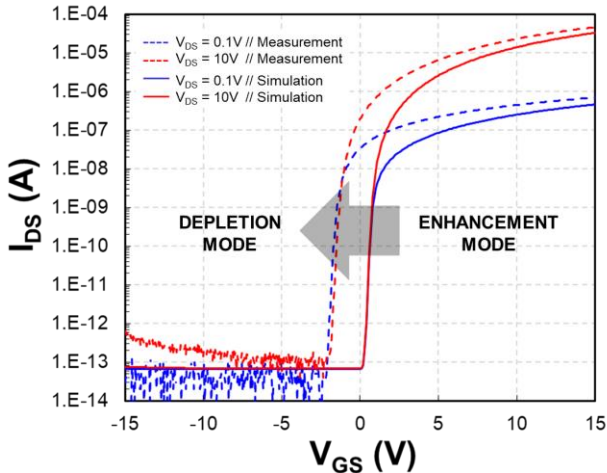

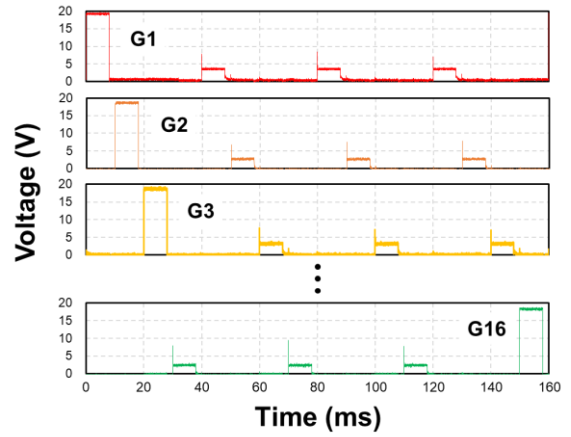**Figure 5.** Transfer curve of a-IGZO TFT (W/L = 10μm/10 μm).

Figure 6. Measurement results of gate output voltage

Fig. 6 shows the gate output voltage of 16 stages. It operates well in sequential order.
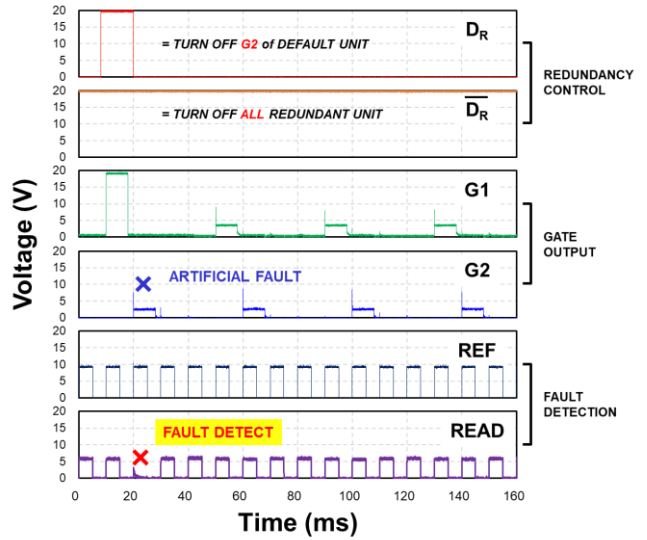

Figure 7. Measurement results of the redundancy control and the fault detection of the proposed circuit.

Fig.7 shows the measurement results of the redundancy control and the fault detection function of the proposed circuit. The high voltage of D_R in the period G1 means turning off G2 of default unit and continuous high voltage of D_R bar means turning off all stage of redundant unit. As a result, the artificial fault was generated in G2. And to detect the location where the fault occurs, the reference signal and the readout voltages were compared. As shown in Fig.7, it was easily concluded that the fault occurs in the G2.

4. Conclusion

In this paper, we proposed the fault-tolerant integrated gate driver circuits. To achieve fault-tolerance, decoder-type gate driver circuit, redundant unit and the fault detection circuit are combined. The function of the proposed circuit is verified by simulation and

fabrication results. We think our proposed circuit can contribute to expanding the lifetime of flexible displays.

5. Acknowledgements

6. References

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